

Figure 1

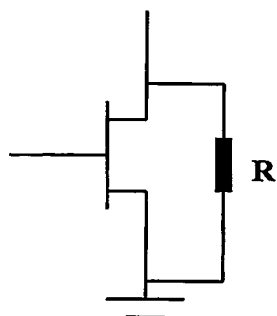


Figure 2

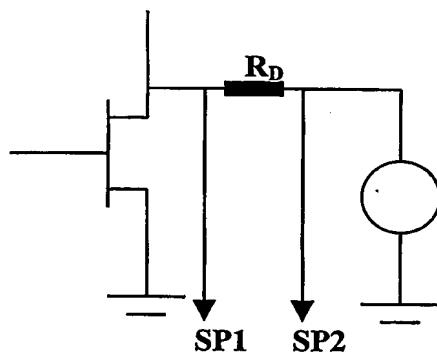


Figure 3

2/7

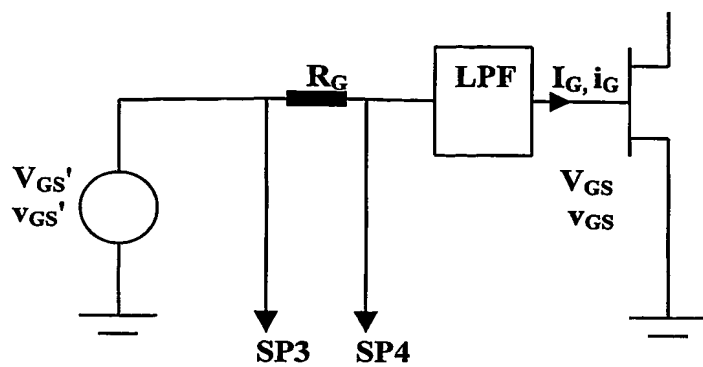


Figure 4

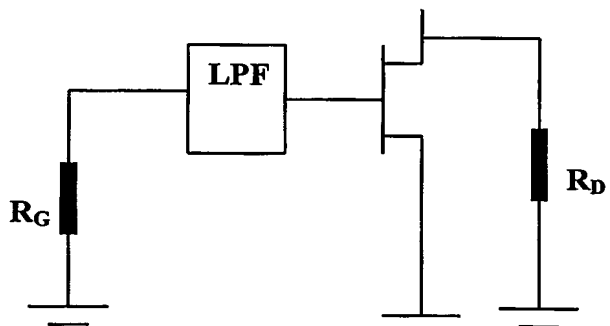
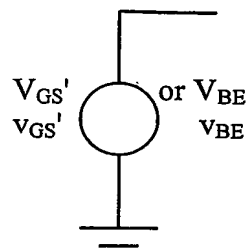


Figure 5

Input generator



Output generator

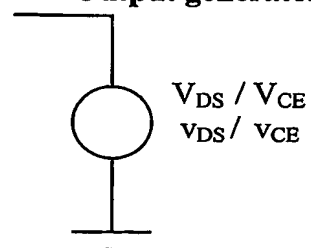


Figure 6

Input op amp

Output op amp

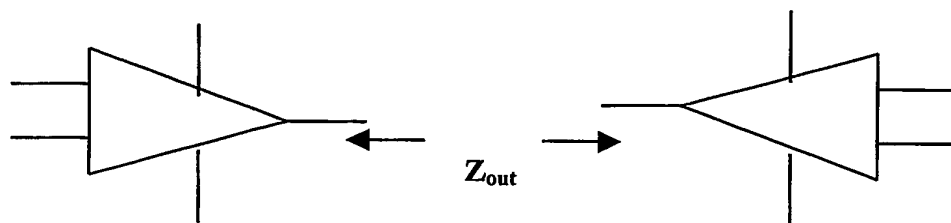


Figure 7

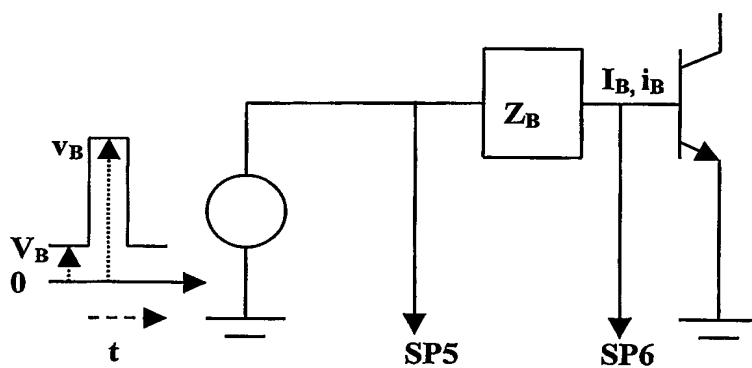


Figure 8

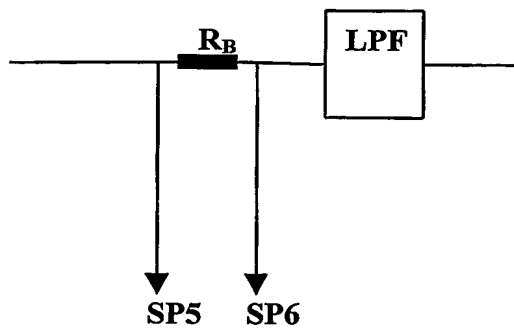


Figure 9

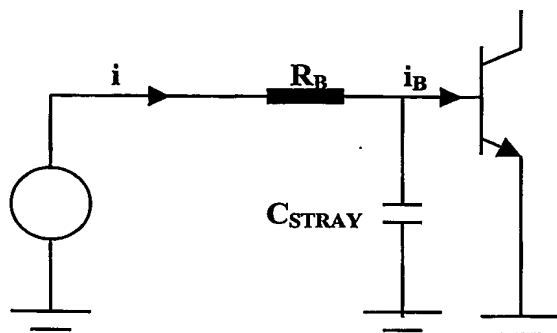


Figure 10

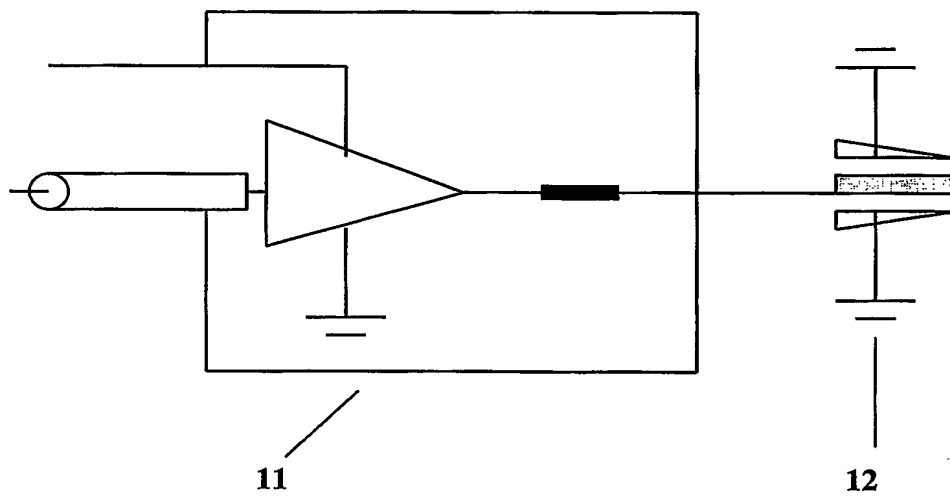


Figure 11

5/7

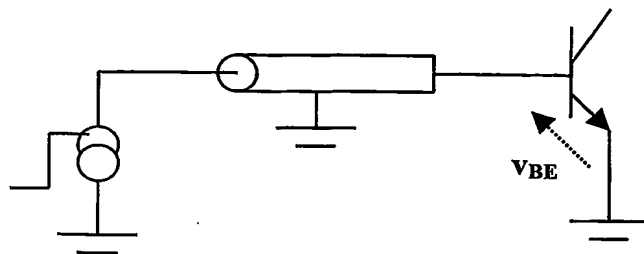


Figure 12

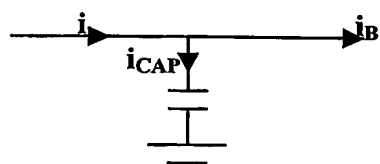


Figure 13

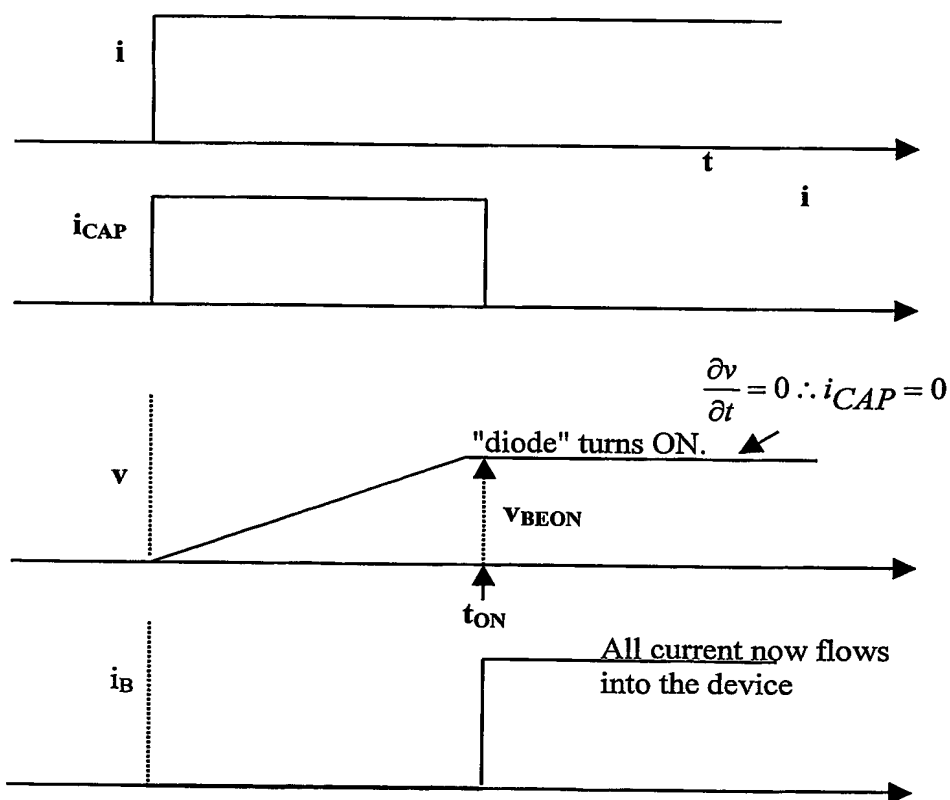


Figure 14

6/7

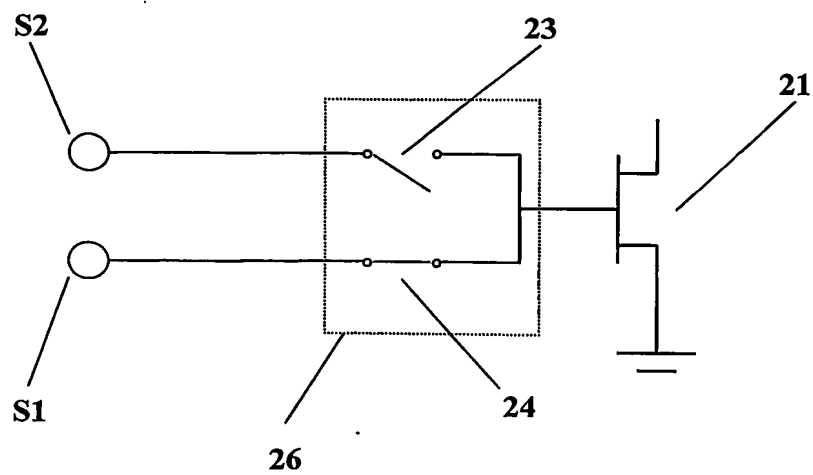


Figure 15

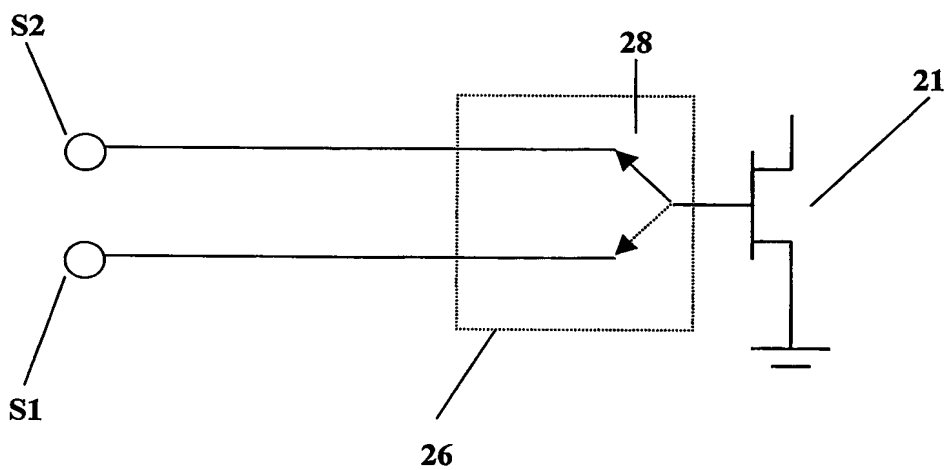


Figure 16

7/7

Figure 17a

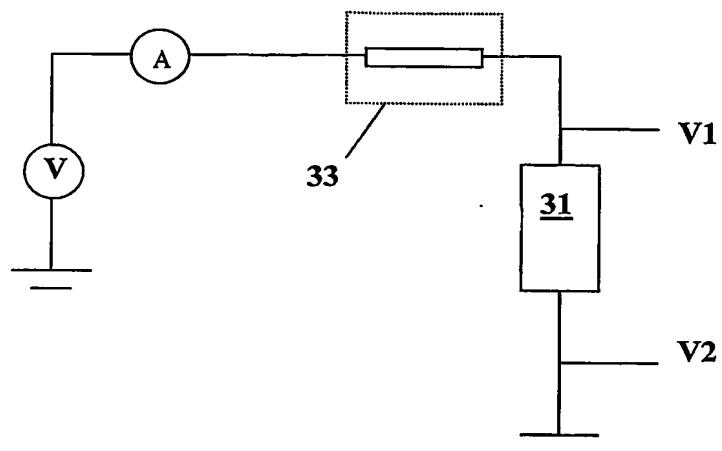


Figure 17b

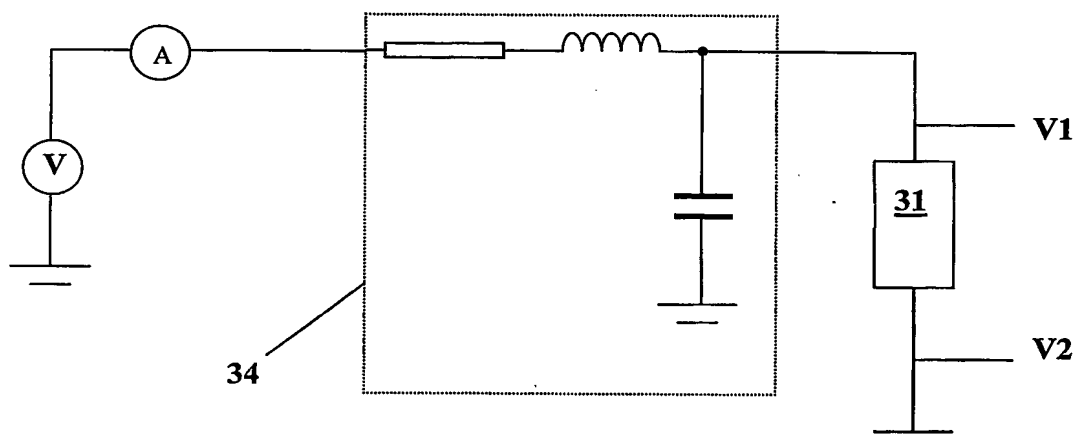


Figure 17c

